

WHAT IS CLAIMED IS:

1. A method of operating a computer system that includes first and second processors and memory shared thereby, the method comprising:
- concurrently executing first and second instructions on respective ones of the first and second processors, the first and second instructions each reserving in a same predefined order plural respective locations of the memory,
- wherein, for at least the first instruction, signaling of a fault corresponding to a later reserved one of the respective locations depends on a value read from an earlier reserved one of the respective locations.
2. The method of claim 1, wherein the predefined order is in accordance with a fixed total order of locations within the memory.
3. The method of claim 1, wherein the predefined order is one of ascending and descending memory address order.
4. The method of claim 1, wherein the reserving includes locking an associated cache-line.
5. The method of claim 1, wherein the reserving locks at least the respective location, but substantially less than all the memory.
6. The method of claim 1, wherein the first and second instructions are linearizable synchronization operations.
7. The method of claim 1, wherein the first instruction is a double compare-and-swap instruction.

1 8. The method of claim 1,
2 wherein the first instruction is a compound compare-and-swap instruction;
3 wherein the respective locations reserved by the compound compare-and-swap
4 instruction number N; and
5 wherein signaling of a fault corresponding to a later reserved one of N
6 locations depends on at least one value read from an earlier reserved
7 one the N locations.

1 9. The method of claim 1,
2 wherein the first instruction is a double compare-and-swap instruction; and
3 wherein, unless a value read from the earlier reserved one of the respective
4 locations compares to a corresponding test value, no fault
5 corresponding to the later reserved one of the respective locations is
6 signaled.

1 10. The method of claim 1,
2 wherein the execution of the first instruction includes access to the earlier
3 reserved one of the respective locations; and
4 wherein, unless the access succeeds, no fault corresponding to the later
5 reserved one of the respective locations is signaled.

1 11. The method of claim 1, wherein the execution of the first instruction
2 includes
3 a first access corresponding to an earlier reserved one of the respective
4 locations; and
5 an optional second access that signals a fault only if the first access succeeds.

1 12. The method of claim 1,
2 wherein the respective locations reserved by the first and second instructions
3 are disjoint; and
4 wherein the concurrent execution is non-blocking.

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1 40. A processor of claim 35,
2 wherein the predefined order is ascending memory address order.

1 41. A processor of claim 35,
2 wherein the predefined order is descending memory address order.

1 42. The processor of claim 35,
2 wherein the first instruction and the corresponding instruction are same
3 instructions.

1 43. The processor of claim 35,
2 wherein the first instruction and the corresponding instruction both implement
3 a compound Compare-and-swap (nCAs) operation.

1 44. An apparatus comprising:
2 a memory store; and
3 means for separately reserving in response to a single instruction, plural
4 locations of the memory store in a predefined order in accordance with
5 a fixed total order of locations in the memory store.

1 45. The apparatus of claim 44, further comprising:
2 a cache,
3 wherein the means for separately reserving includes means for separately
4 locking cache lines associated with each of the plural locations.

1 46. The apparatus of claim 44, further comprising:
2 means for signaling, if at all, a fault corresponding to a later reserved one of
3 the locations based on a result of access to an earlier reserved one of
4 the locations.

1 47. A method of operating a computer system that includes a memory shared
2 by plural processors thereof, the method comprising:
3 in response to execution of a single instruction by one of the processors,

4 separately reserving plural locations of the memory; and
5 signaling a fault corresponding to a later reserved one of the locations
6 based on a value read from an earlier reserved one of the
7 locations.

1 48. The method of claim 47,
2 wherein, unless the value read from the earlier reserved location compares to a
3 corresponding test value, no fault corresponding to the later reserved
4 location is signaled.

1 49. The method of claim 47,
2 wherein the separately reserving includes separately locking at least the plural
3 locations, but substantially less than all the memory.

1 50. The method of claim 47,
2 wherein the computer system further includes cache storage; and
3 wherein the separately reserving includes separately locking respective cache
4 lines associated with the plural locations.

1 51. The method of claim 50,
2 wherein the cache storage includes a coherently maintained set of caches
3 including ones respectively associated with each of the plural
4 processors.

1 52. The method of claim 47,
2 wherein the instruction implements a compound Compare-and-swap (nCAs)
3 operation.

1 53. The method of claim 47,
2 wherein the instruction implements a Double Compare-and-swap (DCAS)
3 operation.

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1 65. The computer program product of claim 63,
2 wherein the instruction further directs the processor to reserve the first and
3 second memory locations in a predefined order in accordance with a
4 fixed total order of memory locations.

1 66. The computer program product of claim 63,
2 wherein, unless the value read compares to a test value, no fault corresponding
3 to the second memory location is signaled.

1 67. The computer program product of claim 63,
2 wherein the instruction is a compound compare-and-swap instruction.

1 68. The computer program product of claim 63,
2 wherein the at least one computer readable medium is selected from the set of
3 a disk, tape or other magnetic, optical, or electronic storage medium
4 and a network, wireline, wireless or other communications medium.

1 69. An apparatus comprising:
2 a memory store;
3 means for accessing in response to a single instruction, first and second
4 locations of the memory store; and
5 means for signaling, if at all, a fault corresponding to the second location
6 based on a value read from the first location.

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